

What is claimed is:

- 1 1. A processor comprising:
2 at least one source location, each source location comprising a validity
3 bit to indicate validity of data in the at least one source location; and
4 a data validity circuit coupled to the at least one source location to
5 determine the validity of the data in the at least one source location, said data
6 validity circuit to indicate the validity of the data, by writing a validity bit in a
7 destination location based upon the validity bit in the at least one source
8 location.
- 1 2. The processor of claim 1 wherein writing a validity bit in a destination location
2 comprises writing a bit in a destination register in the processor to indicate validity of
3 data in the destination location.
- 1 3. The processor of claim 2 further comprising a checker unit coupled to the
2 destination location and to an execution unit.
- 1 4. The processor of claim 3 wherein the checker unit retires instructions from the
2 execution unit.
- 1 5. The processor of claim 3 wherein the checker unit re-schedules instructions for
2 re-execution by the execution unit.

1 6. The processor of claim 3 further comprising a retirement unit coupled to the
2 checker unit to receive instructions that execute with valid data in the destination
3 location.

1 7. The processor of claim 1, wherein the data validity circuit comprises any one of
2 an AND-gate and an OR-gate.

1 8. The processor of claim 1 wherein the source location is any one of a register in
2 the processor, cache, and permanent memory, said register, cache and permanent
3 memory having a bit to indicate validity of data in the register, cache, and the
4 permanent memory.

1 9. The processor of claim 1 wherein the destination location is any one of a
2 register in the processor, cache, and permanent memory, said register, cache, and
3 permanent memory having a bit to indicate validity of data in the register, cache, and
4 the permanent memory.

5 10. An method comprising:
6 writing a bit in one or more source locations, said bit to indicate the validity of
7 the data in each of the one or more source locations;
8 reading the bit to determine the validity of the data in the one or more source
9 locations;
10 writing a bit in a destination location, said bit to determine the validity of the
11 data in the destination location based on the validity of the bit in the one or more source
12 location; and

13 re-scheduling an instruction for execution if the bit in the destination location
14 indicates invalid data.

1 11. The method of claim 10 further comprising retiring the instruction if the bit in
2 the destination location indicates valid data.

1 12. The method of claim 10 wherein reading the bit to determine the validity of the
2 data in the one or more source locations comprise using any one of an OR-gate and an
3 AND-gate to read the bit in the one or more source locations.

1 13. An apparatus comprising:
2 means for writing a bit in one or more source locations, said bit to indicate the
3 validity of the data in each of the one or more source locations;
4 means for reading the bit to determine the validity of the data in the one or more
5 source locations;
6 means for writing a bit in a destination location, said bit to determine the
7 validity of the data in the destination location based on the validity of the bits in the one
8 or more source locations; and
9 means for re-scheduling an instruction for execution if the bit in the destination
10 location indicates invalid data.

1 14. The apparatus of claim 13 further comprising means for retiring the instruction
2 if the bit in the destination location indicates valid data.

1 15. The apparatus of claim 13 wherein the means for reading the bit to determine
2 the validity of the data in the one or more source locations comprises using any one of
3 an OR-gate and an AND-gate to read the bit in the one or more source locations.

1 16. A computer system comprising:
2 a bus;
3 a memory unit coupled to said bus;
4 a processor to execute an instruction, said processor comprising at least one source
5 register, each source register comprising a validity bit to indicate validity of data in the
6 at least one source register; and
7 a data validity circuit coupled to the at least one source register to determine the
8 validity of the data in the at least one source register, said data validity circuit to
9 indicate the validity of the data in a destination register, by writing a validity bit in the
10 destination register based upon the validity of the data in the at least one source
11 register.

1 17. The processor of claim 16 wherein the validity bit is stored contiguous with data
2 bits.

1 18. The processor of claim 16 further comprising a checker unit coupled to the
2 destination register and to an execution unit.

1 19. The processor of claim 18 wherein the checker unit retires instructions from the
2 execution unit.

1 20. The processor of claim 18 wherein the checker unit re-schedules instructions for
2 re-execution by the execution unit.

1 21. The processor of claim 18 further comprising a retirement unit coupled to the
2 checker unit to receive instructions that execute with valid data in the destination
3 register.

1 22. The apparatus of claim 16, wherein the data validity circuit comprises any one
2 of an AND-gate and an OR-gate.

1 23. An article of manufacture comprising:
2 a machine-accessible medium including instructions that, when executed by a
3 machine, causes the machine to perform operations comprising
4 writing a bit in one or more source registers, said bit to indicate the validity of
5 the data in each of the one or more source registers;
6 reading the bit to determine the validity of the data in the one or more source
7 registers;
8 writing a bit in a destination register to determine the validity of the data in the
9 destination register based on the validity of the bits in the one or more source registers;
10 and
11 re-scheduling an instruction for execution if the bit in the destination register
12 indicates invalid data.

1 24. The article of manufacture as in claim 23, further comprising instructions for
2 retiring the instruction if the bit in the destination register indicates valid data.

1 25. The article of manufacture as in claim 23, wherein instructions for reading the
2 bit to determine the validity of the data in the one or more source registers comprises
3 further instructions for using at least one of an OR-function and an AND-function to
4 examine the bit in the one or more source registers.